



## Executive Summary

Oski delivered confidence with an exhaustive formal sign-off for a Qualcomm high-performance mobile GPU's critical IPs. Result was a state-of-the-art multi-client, multi-bank memory cache subsystem, free from corner-case deadlocks in design time.



Exhaustive Formal Sign-Off



Found All Deadlock Bugs

## About Qualcomm

Qualcomm is a global leader in the development and commercialization of foundational technologies that help power the modern mobile experience. From network equipment and broadband gateway equipment to consumer electronic devices, Qualcomm helps billions of people around the world connect, compute and communicate.

Reference: DAC 2020, "[Proving Absence of Deadlock in High-Performance Cache Sub-Systems](#)"; Vaibhavi Solanki, Qualcomm

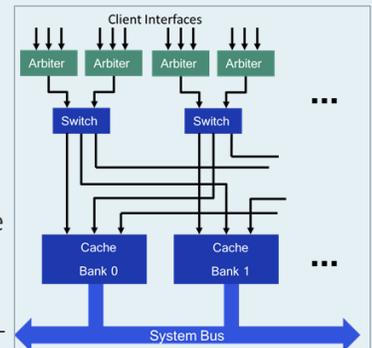
## Challenge

In a recent mobile GPU design, Qualcomm's performance optimizations included techniques for maximizing system throughput for multiple IP Clients accessing multiple, shared Cache Banks via Switches. The design allows transaction requests to proceed in out-of-order to the Cache Banks, but the responses must be presented back to Clients in order.

This approach introduces multiple types of critical deadlock risk, as the Switch response buffers can become full while waiting to receive the response to earlier requests. Verifying such dead-lock conditions, with the multitude of traffic scenarios and design parameters (burst size, target cache bank, etc.), proves to be too expansive for traditional simulation in project time.

## Solution—Exhaustive Formal Sign-Off

Oski worked closely with Qualcomm to execute a Level 4 exhaustive formal sign-off of this high-risk memory cache subsystem block. This was made possible by first building an abstraction model for the switch, allowing configurability and scalability with the number of switches. Also developed was a formal testbench that scales in the same way. This robust framework allowed the team to overcome proof complexity and lead to the exhaustive verification of complex sequences of input requests to the system which triggered corner case deadlock bugs.



In one example of a bug that could not have been discovered with simulation in project time, the preconditions to trigger the bug were:

- Each of two Clients must send three burst transactions directed towards two Cache Banks in the system through a single switch
- Client A sends the first request to Bank 1 and the next two requests to Bank 0
- Client B sends the first request to Bank 0 and the next two requests to Bank 1
- The timing of requests is such that the transaction streams arriving at both Cache Banks to go out-of-order by 2 requests

When these conditions arise, the responses from the Cache Banks to the out-of-order transactions fill up the buffers in the Switch, which blocks the responses from the first set of transactions when they become available. The Switch must send responses for the first transactions back to the Clients before freeing up any room in the buffers, so the entire system is then deadlocked.

## Results

Oski delivered exhaustive formal sign-off of the Cache subsystem and found all corner-case deadlock bugs, which were not possible to find in project time with only simulation. In the end, Oski proved the absence of deadlock in the fixed design and delivered the confidence required for tape out.