Case Study: Microchip PCIe Network IC

Executive Summary

Oski delivered confidence with an exhaustive Level 4 formal sign-off for a Microchip PCIe Gen 4 high-risk Rx path IP. Result was a robust implementation, identifying 14 simulation-resistant bugs in design time and proving that the last bug was found.

Exhaustive Formal Sign-Off

14 Simulation-Resistant Bugs Discovered

About Microchip

Microchip Technology Incorporated is a leading provider of smart, connected and secure embedded control solutions. Its easy-to-use development tools and comprehensive product portfolio enable customers to create optimal designs, which reduce risk while lowering total system cost and time to market.

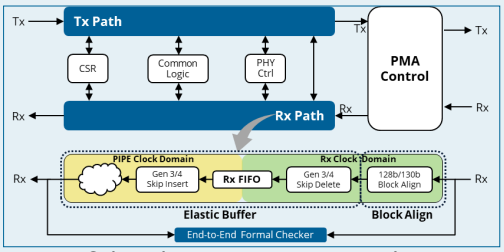
Reference: Decoding Formal Club, December 2019, "Metrics-Driven Formal Sign-Off of PCIe PCS", Maysam Mirahmadi, Microchip

Challenge

Microchip's PCIe Gen 4 network IC offers high-bandwidth connectivity between CPUs and peripherals like GPUs and SSDs. For high throughput, it features 16 lanes for Tx and Rx traffic. The design's PCIe PCS (Physical Control Subsystem) block was identified as a high-risk block. Within the PCS, the Tx path has a well-characterized state space as a transaction initiator, lending itself well to verification via simulation.

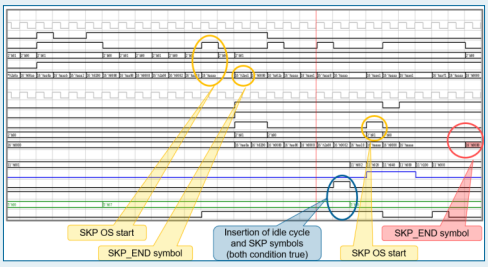
In contrast, as a target the Rx path is a more complex due to responsibility of transaction robustness, namely for identifying information ("Block Align"); detecting, reporting, and recovering from framing errors; as well as buffer management across two similar but different clock domains (PIPE and Rx in the "Elastic Buffer"). This architecture leads to simulation resistance, as there are just too many permutations of clock edges, ordered sets and sequences, and modes (Gen 3/4/loopback/etc.) to test in project time.

Solution—Exhaustive Formal Sign-Off



Oski collaborated with Microchip to execute a Level 4 exhaustive formal sign-off of the PCIe PCS Rx path block. This was done by building an abstraction model and formal testbench for two DUTs for the receiver, Elastic Buffer and Block Align. Oski verified the elasticity of the Elastic Buffer with proof of absence of data loss/corruption, and set up an environment to verify all possible sequences of clock edges for Rx and PIPE clocks. Additionally, the abstractions allowed efficient implementation and convergence of checkers in the verification plan.

One example of a critical, data corruption bug which was discovered is shown here. The bug is simulation-resistant because it is triggered only when Skip Ordered Set insertion and Idle Cycle insertion, both very rare events, collide with specific timing. Furthermore, the last SKP symbol must be aligned to the least-significant word of the bus to cause the failure.



Formal sign-off not only caught this corner case, but delivered exhaustive coverage required to test all permutations of input stimuli, including all types/sequences of PCIe ordered sets and framing tokens.

Results

Oski delivered exhaustive Level 4 formal sign-off of the PCIe Gen 4 PCS Rx block and found 14 bugs, which were not possible to find in project time with only simulation. In the end, Oski achieved formal sign-off for all modes and proved that the last bug had been found, which delivered the confidence required for tape out.

Formal Sign-Off. Delivered.

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